Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **N. 1G**
2. **1A**
3. **1B**
4. **1Y0**
5. **1Y1**
6. **1Y2**
7. **1Y3**
8. **GND**
9. **2Y3**
10. **2Y2**
11. **2Y1**
12. **2Y0**
13. **2B**
14. **2A**
15. **N. 2G**
16. **VCCVCC**

**.055”**

**14 13 12 11 10**

**9**

**8**

**8**

**7**

**15**

**16**

**16**

**1**

**2**

**3 4 5 6**

**MASK**

**REF**

**AC 139**

**.068”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004 x .004”**

**Backside Potential: VCC or FLOAT**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .055” X .068” DATE: 8/25/21**

**MFG: SILICON SUPPLIES THICKNESS .014” P/N: 54AC139**

**DG 10.1.2**

#### Rev B, 7/1